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High-k Gate Stacks on Low Bandgap Tensile Strained Ge and GeSn Alloys for Field-Effect Transistors

Stephan Wirths,*[,†] Daniela Stange,[†] Maria-Angela Pampillón,[†,‡] Andreas T. Tiedemann,[†] Gregor Mussler,[†] Alfred Fox,[†] Uwe Breuer,[§] Bruno Baert,[∥] Enrique San Andrés,[‡] Ngoc D. Nguyen,[∥] Jean-Michel Hartmann,[⊥,△] Zoran Ikonic,[#] Siegfried Mantl,[†] and Dan Buca*[,†]

[†]Peter Grünberg Institute (PGI 9) and JARA-FIT, Forschungszentrum Jülich, 52425 Jülich, Germany

[‡]Departamento Física Aplicada III: Electricidad y Electrónica, Universidad Complutense de Madrid (UCM), 28040 Madrid, Spain

[§]Central Institute for Engineering, Electronics and Analytics (ZEA), Forschungszentrum Jülich, 52425 Jülich, Germany

[∥]Department of Physics, Solid State Physics - Interfaces and Nanostructures, Université de Liège, B-4000 Liège, Belgium

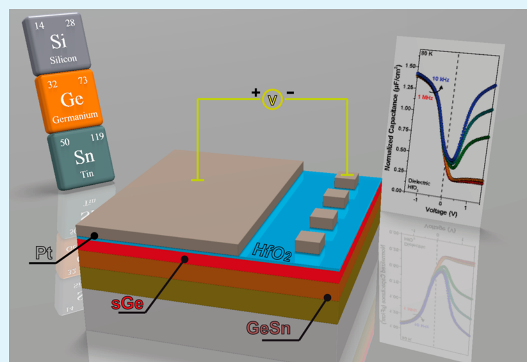
[⊥]Université Grenoble Alpes, 38000 Grenoble, France

[△]LETI, Minatec Campus, CEA, 17 rue des Martyrs, 38054 Grenoble, France

[#]Institute of Microwaves and Photonics, School of Electronic and Electrical Engineering, University of Leeds, Leeds LS2 9JT, United Kingdom

Supporting Information

ABSTRACT: We present the epitaxial growth of Ge and $Ge_{0.94}Sn_{0.06}$ layers with 1.4% and 0.4% tensile strain, respectively, by reduced pressure chemical vapor deposition on relaxed GeSn buffers and the formation of high-k/metal gate stacks thereon. Annealing experiments reveal that process temperatures are limited to 350 °C to avoid Sn diffusion. Particular emphasis is placed on the electrical characterization of various high-k dielectrics, as 5 nm Al_2O_3, 5 nm HfO_2, or 1 nmAl_2O_3/4 nm HfO_2, on strained Ge and strained $Ge_{0.94}Sn_{0.06}$. Experimental capacitance−voltage characteristics are presented and the effect of the small bandgap, like strong response of minority carriers at applied field, are discussed via simulations.



KEYWORDS: *strained Ge, GeSn, high-k dielectrics, low bandgap alloys, field effect transistor*

Recently, germanium and germanium−tin (GeSn) have attracted great interest to integrate nanoelectronics and photonics to realize high energy-efficient circuits. Ge offers the highest bulk hole mobility among all semiconductors.[1,2] Its integration into microelectronics was hindered mainly because of the poor structural and electrical properties of the high-k/Ge interface. Recent work on surface passivation of bulk Ge crystals[3,4] and gate dielectric deposition on those surfaces[5,6] has paved the way toward the integration of Ge into high performance metal oxide semiconductor field effect transistors (MOSFETs). Low bandgap semiconductors with a direct gap are particularly desired for novel low power devices such as tunnel-field effect transistors (tunnel-FET).[7,8] In this context, the electronic band structure of Ge can be tuned by applying biaxial tensile strain[9] or by Sn alloying[10] toward a fundamental direct bandgap which enhances the tunneling probability and thus the ON-current of tunnel-FETs.[8,11,12] Vertical tunnel-FET structures using strained Ge channels were recently proposed based on InGaAs[13] and GeSn[11] buffer substrates. Under biaxial strain both the indirect (L-valley) as well as the direct (Γ-valley) bandgap shrink significantly and Ge becomes direct at a strain level of about 1.5%. The alloying with Sn shifts the direct transition to lower tensile strains. In addition to a direct bandgap, strained GeSn layers offer smaller effective masses for both, holes and electrons,[14] making their use advantageous for drift-based devices as MOSFETs. Tensile biaxial strain in Ge and GeSn alloys is very promising; however, its experimental implementation using a simple and Si-based compatible process is challenging. The breakthrough in the growth of high-quality epitaxial GeSn[15,16] and SiGeSn[17,18] alloys enables a new degree of freedom in group IV strain engineering.

On the basis of these achievements, a study of high-k/metal gate stacks on tensile strained Ge and GeSn alloys on appropriate buffers and their epitaxial growth is presented. Furthermore, the thermal stability of these novel materials is reported as this is most relevant for future device developments. Different high-k dielectrics have been deposited in order

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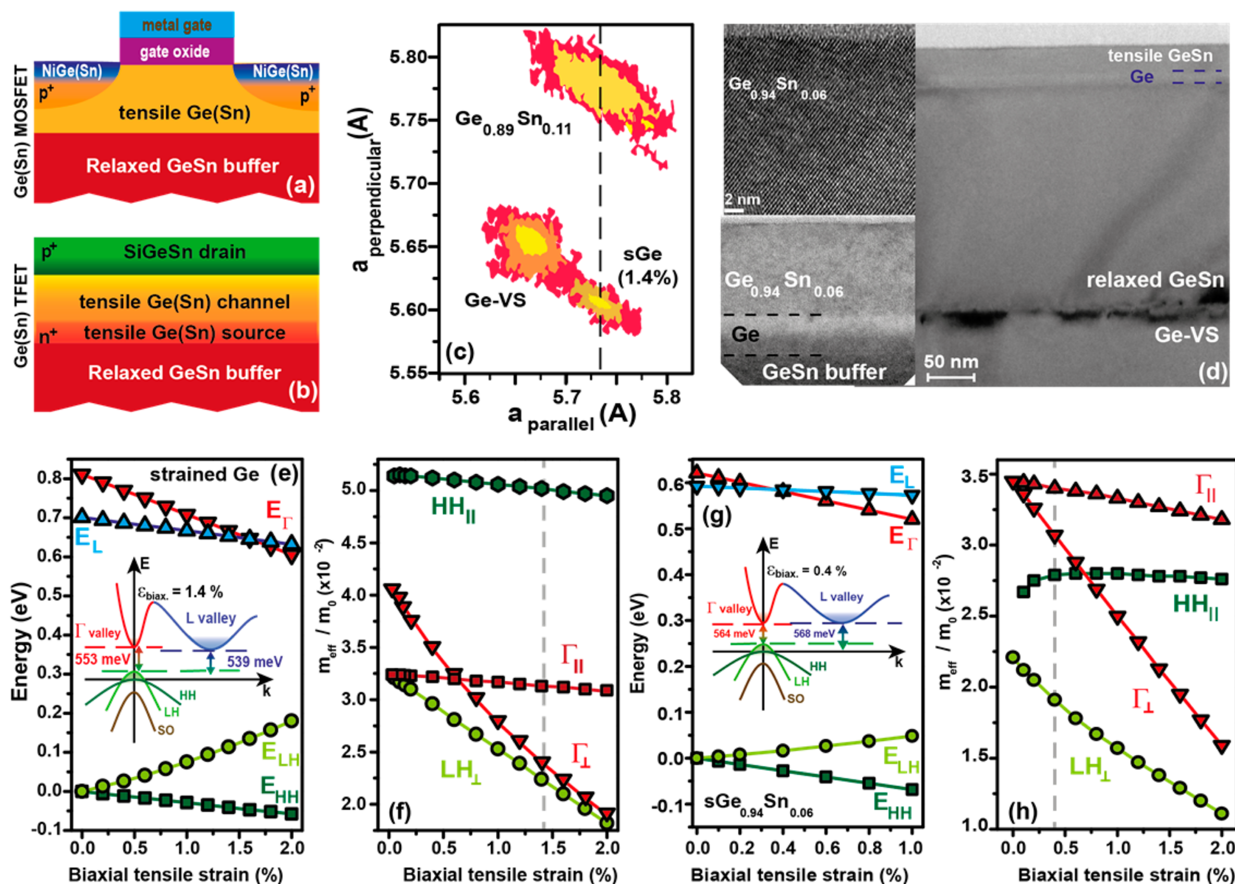

Figure 1. Schematics of possible (a) MOSFET and (b) TFET devices based on tensile strained Ge(Sn) layers. (c) XRD RSM of strained Ge/GeSn/Ge-VS heterostructures indicating 1.4% biaxial tensile strain in the top Ge layers. (d) TEM micrographs of the strained $Ge_{0.94}Sn_{0.06}$/Ge/$Ge_{0.89}Sn_{0.11}$/Ge-VS structure. The inset shows the high crystallinity of the top GeSn layer. (e–h) Effect of biaxial strain on the (e, g) electronic band structure and (f, h) electron and hole effective masses at 300 K. The schematic band structure of Ge and GeSn under tensile strain of 1.4% and 0.4%, respectively, are shown as inset.

to study the interface passivation via electrical measurements at temperatures ranging from 80 to 300 K.

Ge/GeSn heterostructures were grown in an industry compatible AIXTRON TRICENT reduced-pressure chemical vapor deposition reactor on 2.5 μm thick Ge virtual substrates (VS) on 200 mm Si(100) wafers. The Ge-VS exhibits a weak tensile strain of about 0.16% and a threading dislocation density close to 1×10^7 cm^{-2}. Partially relaxed GeSn layers with thicknesses between 200 and 300 nm were grown on top of these Ge-VS and capped with 50 to 70 nm thick Ge layers. A schematic of a MOSFET with a tensile strained Ge channel and source/drain NiGe(Sn) stressors as well as a possible layer structure of p-i-n Tunnel-FET with strained Ge and GeSn alloys are shown in Figure 1a, b.

The biaxial tensile strain in the Ge epilayer increases with the Sn concentration and the degree of strain relaxation of the GeSn buffer. Different Ge strains, namely 0.7, 1.1, and 1.4%, were achieved by modifying the Sn content in the buffer (details in S.I.). The X-ray diffraction (XRD) reciprocal space map (RSM) of 70 nm thick 1.4% strained Ge on 300 nm $Ge_{0.89}Sn_{0.11}$/ Ge-VS heterostructure is shown in Figure 1c. It is obvious that this GeSn buffer technology facilitates complex strained heterostructures adaptable for specific devices designs. A transmission electron microscope (TEM) image of such a heterostructure consisting of 30 nm tensile strained $Ge_{0.94}Sn_{0.06}$ layer with a 10 nm strained Ge layer to separate the top tensile $Ge_{0.94}Sn_{0.06}$ from the compressive $Ge_{0.09}Sn_{0.11}$ buffer is presented. The TEM images prove the high quality of the 0.4% tensile strained $Ge_{0.94}Sn_{0.06}$/Ge/$Ge_{0.89}Sn_{0.11}$ buffer/Ge-VS structure with no indication of defects, such as threading dislocations, related to strain relaxation of the strained top layers.

Figure 1e–h shows the Ge and $Ge_{0.94}Sn_{0.06}$ bandgaps and the electron and hole effective masses at 300 K as a function of strain, as calculated with the 8 × 8 k.p method including strain.[19] The biaxial strain lifts the degeneracy of heavy-hole (HH) and light-hole (LH) valence bands, hence the LH band population increases. The Γ-valley electron and the LH band effective masses decrease with increasing tensile strain.

In the following, we present the formation of high-*k* dielectric stacks on strained Ge(Sn) /GeSn heterostructures and corresponding metal oxide semiconductor (MOS) capacitors, an essential ingredient of MOSFETs. After diluted "HF:HCl-last" wet cleaning step the strained Ge(Sn) samples were loaded into an atomic layer deposition reactor where three different high-k dielectric stacks were deposited: 5 nm Al_2O_3, 1 nm Al_2O_3/4 nm HfO_2, or 5 nm HfO_2 (details in the Supporting Information) In addition, a 5 min in situ O_3 dry oxidation step was performed before or after the deposition of the first 1 nm Al_2O_3. The O_3 dry oxidation produces a controlled interfacial GeO_x growth which improves the Ge surface passivation.[20] The MOS capacitor formation is completed by the deposition of Pt

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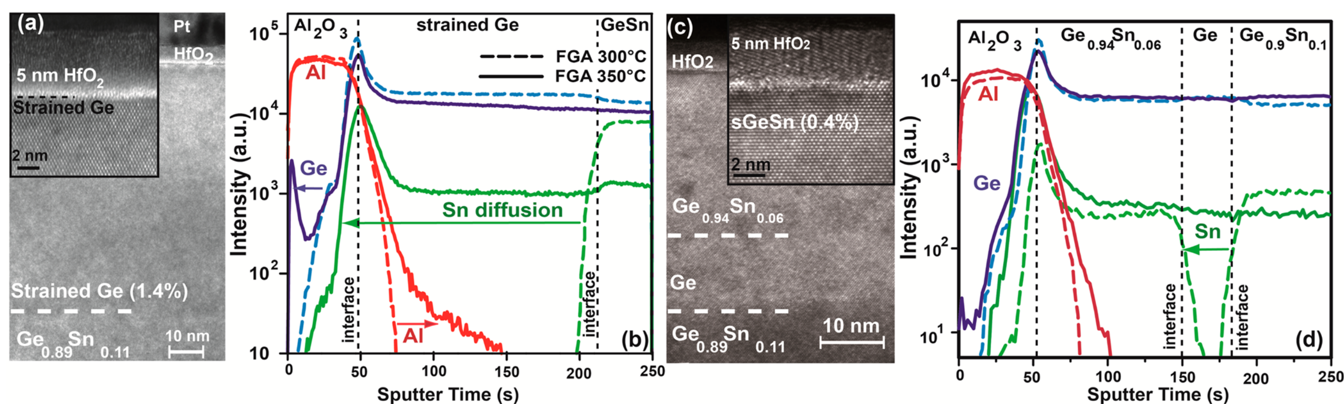

Figure 2. (a, c) TEM micrographs of the 5 nm HfO_2/strained Ge(Sn)/$Ge_{0.89}Sn_{0.11}$/Ge-VS structures. The insets in shows the interface HfO_2/strained Ge(Sn) with the thin interface layer (~0.8 nm) formed during the O_3 oxidation. (b, d) ToF-SIMS spectra of Al_2O_3/strained Ge/$Ge_{0.905}Sn_{0.095}$ after FGA at 300 °C (dashed lines) and 350 °C (solid line). At 350 °C Ge diffuses to the surface, whereas Sn diffusion stops within the dielectric layer.

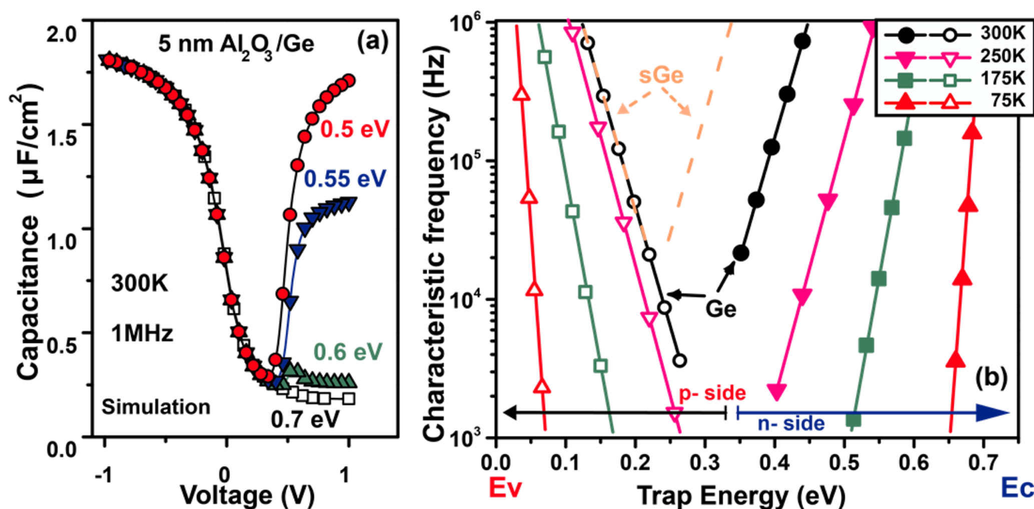

Figure 3. (a) $C-V$ simulations for Al_2O_3/Ge using Ge bandgap as parameter. (b) Calculated resonance frequency of trap levels in Ge for different temperatures and for Ge with strain level of 1.1%. The temperature dependence of the effective density of states, bandgap, and electron thermal velocities are calculated using data from ref 25. The data for strained Ge (thick dashed lines) refer only to 300 K. Ge bulk parameters are used.

as metal contact and forming gas annealing (FGA) at different temperatures (300–400 °C) for 10 min in H_2 (4%)/N_2(96%) ambient.

The thermal stability of the strained heterostructures was investigated prior to electrical characterization. Because of the low solid solubility of Sn in Ge, Sn tends to segregate toward the surface in metastable GeSn layers.[21] Hence, we investigated MOS structures at different FGA temperatures. Figure 2b, d shows elemental time-of-flight secondary ion mass spectroscopy (ToF SIMS) depth profiles for Al_2O_3 capped strained Ge and strained GeSn heterostructures annealed at 300 °C (broken lines) and 350 °C (solid lines). For the FGA at 300 °C the Sn signals (green dashed line) indicate homogeneous Sn distribution within the GeSn layers, with sharp Ge/GeSn interfaces. Only moderate Ge diffusion (blue dashed line) into Al_2O_3 layers is observed. XRD-RSM measurements confirmed that the lattice constant remained unchanged during this FGA; i.e., full elastic strain is conserved. Increasing the FGA temperature to 350 °C induces strong diffusion of Sn from the GeSn layers into the strained Ge layer reaching the Al_2O_3 (see also S.I.). Detailed analyses of all Ge and Sn isotopes proved that Ge reaches even the high-k surface, while Sn stops within the dielectric layer. In conclusion, at 300 °C Sn diffusion is sufficiently slow to preserve the chemical purity of the Ge layer and the initial strain. Therefore, for all MOS capacitors the deposition of both, Al_2O_3 and HfO_2 dielectrics, the O_3 oxidation and the FGA were performed at 300 °C. The TEM images in Figure 2a, c show both the strained Ge and GeSn MOS capacitors formed with 5 nm HfO_2 dielectric after FGA annealing at 300 °C. The crystalline quality of the layer is conserved and a smooth interface strained Ge(Sn)/HfO_2 observed. High-resolution TEM images allow the estimation of an interface layer of about 0.8 nm.

In the following, we address the challenges due to the very low bandgap in respect of correct electrical characterization of the tensile Ge(Sn)/high-k MOS capacitors. Calculation of the ideal $C-V$ characteristics with a custom-made numerical tool[22] allows assessing the effect of the bandgap energy on the inversion response. Figure 3a shows that inversion response occurs at smaller applied bias and strongly increases with the decrease in the bandgap. Moreover, for smaller bandgaps, e.g., ~0.54 eV, as for 1.4% tensile strained Ge, the inversion response is very strong even at high frequency (1 MHz). The minority carrier response causes severe imprecisions of the

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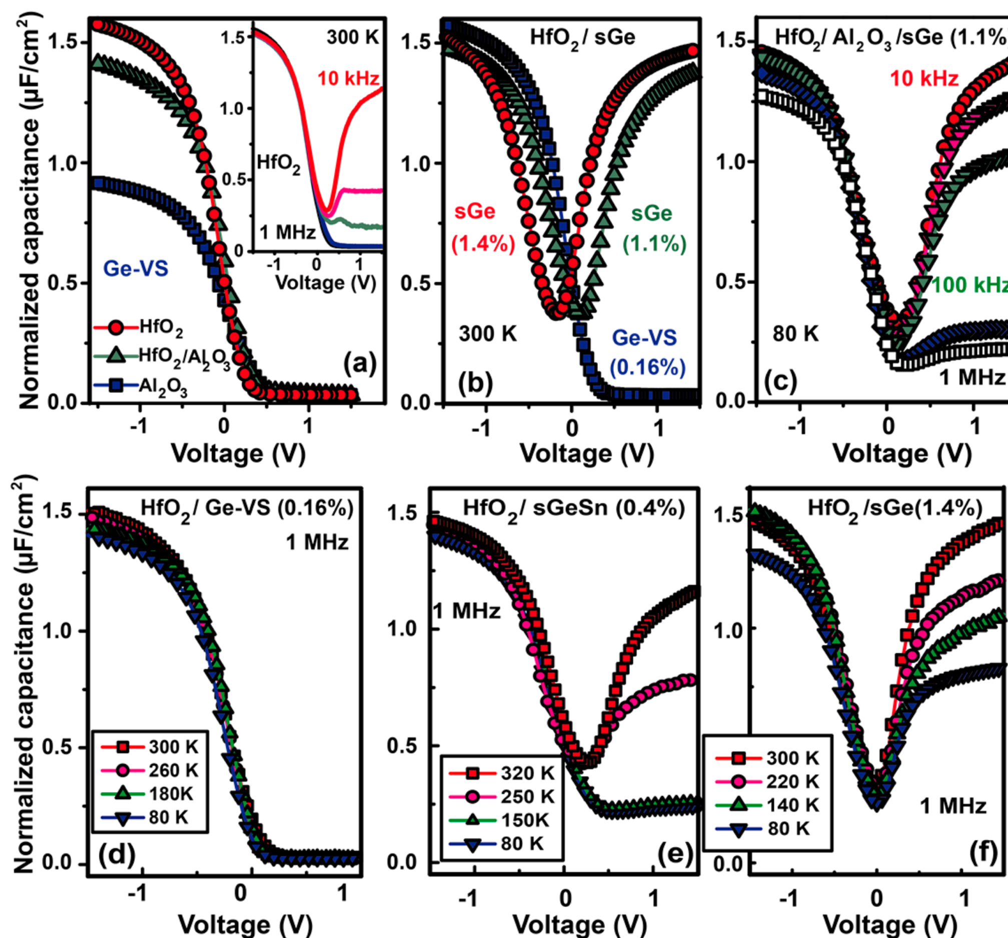

Figure 4. (a) $C-V$ curves of different high-k stacks on Ge-VS measured with 1 MHz at 300 K. The frequency dispersion for HfO_2/Ge-VS is shown as inset; (b) comparison of $C-V$ at 1 MHz for 5 nm HfO_2 on Ge-VS and on 1.1% and 1.4% strained Ge, respectively. (c) Effect of frequency on the $C-V$ response for 1 nm Al_2O_3/4 nm HfO_2/ Ge (1.1% strain) structure at 80 K. (d−f) Temperature dependence of 1 MHz $C-V$ characteristics for 5 nm HfO_2 on (d) Ge-Vs, (e) strained GeSn (0.4%), and (f) strained Ge (1.4%).

conductance methods for the determination of the density of interface traps (D_{it}).[23] The effect of thermal carrier generation can be suppressed at low temperatures. The resonance frequency of a trap level, given by Fermi−Dirac statistics, depends mostly on the energy difference with the band edges and on temperature.[24] Figure 3b shows the resonance frequencies of trap levels in Ge calculated by taking into account the temperature dependence of the effective density of states of the conduction and the valence bands, the variation of the Ge bandgap and of the electron thermal velocity. The dashed lines represent the estimated characteristic trap frequency for 1.1% strained Ge using bulk Ge parameters.[25] The trap energy regions within the bandgap which can be scanned using the standard 1 kHz−1 MHz instrumental frequency range, becomes narrow and shift toward the band edge energy when the measurement temperature is decreased. The above discussion states that for strained Ge and GeSn semiconductors the extraction of D_{it} is not straightforward as for the case of Si or SiGe alloys.

For each strained Ge(Sn)/high-k combination, a comparison was made with reference MOS structures on Ge-VS using identical conditions. The intrinsic carrier concentration in GeSn buffers estimated via electrochemical capacitance voltage measurements is at 1×10^{17} cm^{-3}. In Figure 4a, the room-temperature capacitance−voltage ($C-V$) measurements at modulation frequency of 1 MHz are displayed for three differently processed Ge-based MOS structures.

As expected, the highest capacitance in accumulation, at the same oxide thickness of 5 nm, is obtained for HfO_2 because of a higher effective dielectric constant compared to the Al_2O_3 and Al_2O_3/HfO_2 stacks. For the investigated gate stacks neither humps, due to interface traps, nor frequency-dependent flatband voltage (V_{FB}) shifts, stemming from a high $D_{it,}$ were observed. Although the conductance method is well-suited to quantify the D_{it} at the high-k/semiconductor interfaces when the admittance is governed by the majority carrier response,[26,27] attention has to be paid to the large minority carrier density in Ge,[28] as discussed above. Thus, our extracted D_{it} levels at room temperature of about 1×10^{12} cm^{-2} eV^{-1} for 5 nm Al_2O_3 and 5×10^{12} cm^{-2} eV^{-1} for 5 nm HfO_2 on Ge should be considered as upper limits because of the interaction of interface traps with majority as well as minority carriers[35].

Figure 4b shows that for 1.4% strained Ge MOS capacitors, an inversion capacitance close to the accumulation capacitance is obtained at 300 K at high frequency of 1 MHz. With increasing strain in Ge, the weak inversion (minority carriers) appears before the depletion (majority carriers). This effect has already been reported in literature for cubic Ge.[28] Inversion emerges at smaller applied bias and becomes stronger with the decrease of bandgap, e.g., with an increase in strain in the Ge layer. Moreover, the carriers are able to follow the external

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applied field over the complete frequency range typically used in CMOS characterization. This is a characteristic of low bandgap materials, as strained Ge(Sn) and represents one of the findings of our investigations. In applications, low gate voltages allow reduced losses in electronic circuits because less energy is required to switch the MOSFET devices.

The temperature dependence of the *C*−*V* characteristics for HfO_2 based gate stacks is shown in Figure 4c−f. At lower temperatures the reduced inversion response qualitatively translates into a steeper depletion slope. As explained above, D_{it} data extraction is restricted to a range of energies shifted close to the band edge, over which conductance data can be obtained. At 80 K, the conductance method provides minimum values for D_{it} of $4.1{-}6 \times 10^{12}$ eV^{-1} cm^{-2} for HfO_2 on strained Ge under 1.1% strain as well as a very low D_{it} of $2.9{-}4 \times 10^{12}$ eV^{-1} cm^{-2} for strained GeSn MOS capacitors. For the determination of D_{it} the capture cross-sections and thermal velocities of unstrained Ge were used. To estimate D_{it} at 300 K, we applied the low-frequency method.[29] A minimum D_{it} of 2×10^{12} eV^{-1} cm^{-2} for Ge and ∼ of 5×10^{12} eV^{-1} cm^{-2} for strained Ge under 1.1% and 1.4% was found. The semiconductor bandgap increases with decreasing temperature. The direct bandgap energy of Ge is about 0.8 eV. When the temperature drops from 300 to 80 K, the bandgap energy of bulk Ge increases by about 0.07 eV. Applying the Ge temperature dependence of the bandgap to strained Ge, we obtain the same *C*−*V* characteristics for the 1.1% strained Ge (Figure 4c) and strained GeSn (Figure 4e) at 80 K close to the Ge at RT. Correspondingly, for 1.4% biaxial tensile strained Ge the bandgap energy increases from 0.54 to 0.63 eV from 300 to 80 K. As a consequence, the inversion response should be less pronounced than the one shown in Figure 4f. In order to gain understanding of the inversion response we have performed numerical *C*−*V* simulations including a diffusion model[22,30] of the MOS structures (details in the Supporting Information). The modeling indicates that at constant bandgap but different carrier mobilities the inversion response increases with higher electron (minority carriers) mobility, whereas the hole (majority carriers) mobility has no effect. Consequently, the differences in the inversion response are an indication of enhanced electron mobility under tensile strain, in addition to the bandgap narrowing effect. This is also supported by the effective mass calculation presented in Figure 1f, h, indicating a lower electron effective mass (here minority carriers) in strained Ge as compared with the strained GeSn, for the strain values discussed here. The lowest electron effective mass is calculated for 1.4% strained Ge which shows also experimentally the highest inversion response (see also Table S2 from Supporting Information.). Strained GeSn with very low hole effective masses may be exploited in p-type GeSn channel MOSFETs or tunnel-FETs by forming a strained Ge/strained GeSn source-channel tunneling junction as suggested in Figure 1a.

In summary, epitaxial growth of device-grade Ge and GeSn layers with high tensile biaxial strain up to 1.4% have been achieved by employing high Sn content GeSn buffer layers. Smooth and steep MOS C−V characteristics for Al_2O_3/HfO_2 high-k gate stacks have been demonstrated for the temperature range of 80 to 300 K. Strain induced bandgap narrowing in these low band gap materials results in a strong inversion response of the minority carrier as further substantiated by simulation. Further investigations are needed to elucidate experimentally the carrier transport in these novel materials. The dielectric/strained Ge(Sn) characterization presented here represents an essential step toward realization of Ge(Sn)-MOSFETs In addition, these new semiconductors will inspire novel developments, such as strained Ge(Sn) tunnel-FETs[8] and optoelectronic applications.

■ ASSOCIATED CONTENT

Supporting Information

Details about the characterization of strained Ge(Sn)/GeSn are given, including RSM images and SIMS profiles. The methods used for band structure calculations and simulation of the CV characteristics are also included. This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Authors

*E-mail: s.wirths@fz-juelich.de.

*E-mail: d.m.buca@fz-juelich.de.

Notes

The authors declare no competing financial interest.

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